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FOR

ON-DIE TERMINATION RESISTOR WITH ANALOG COMPENSATION

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ON-DIE TERMINATION RESISTOR WITH ANALOG COMPENSATION

FIELD OF THE INVENTION

The present invention is directed to electrical circuits on printed circuit boards. More particularly, the present invention is directed to analog on-die termination resistors for electrical circuits on printed circuit boards.

BACKGROUND INFORMATION

Printed circuit boards ("PCBs") populated with silicon chips typically require termination resistors for terminating the transmission lines that run throughout the PCBs. Termination resistors are necessary for good signal integrity at a high frequency operation.

Termination resistors can be integrated within the silicon chips or placed directly on the PCB. Traditionally, the termination resistors are placed on the PCB board because of the difficulties in designing high quality resistors in a silicon chip. However,

as electronic systems on PCBs become more and more complicated, there is a large number of input receivers/output drivers that need termination, and consequently it has becomes very difficult to place all of the termination resistors on PCB board. Therefore, the need for the termination resistors to be placed on silicon chips, as on-die termination ("ODT") resistors, has increased.

To compensate for the resistance change caused by process and temperature variations, digital compensation circuits have been used to make sure an ODT resistance is within a pre-determined range over different process corners (i.e., statistical variation process parameters) and temperature. Difficulties arise, however, because the device parameters in these circuits greatly vary with process and temperature conditions, and because the I-V characteristics of MOS transistors used in these circuits are non-linear.

To improve the linearity of an ODT resistor, a number of structures have been explored, including an all-PMOS active resistor structure disclosed in J. Griffin et al., "*Large Signal Active Resistor Output Driver*", IEEE 42nd Symposium on Circuits and Systems (August 8-11, 1999), hereinafter "Griffin". Fig. 1 is a circuit diagram of the active ODT resistor 10 disclosed in Griffin. ODT resistor 10 includes positive-channel metal-oxide semiconductor ("PMOS") transistors 12-14. With resistor 10, the size (i.e., the channel width/channel length ratio) of transistors 12 and 13 are the same, but the size of transistor 14 must be approximately four times the size of transistors 12 and 13 to achieve linearity.

The all-PMOS ODT resistor shown in Fig. 1 has good linearity when used in

digital compensation circuits where the gate bias V_{GG} of transistor 12 at terminal 17 is set to V_{SS}. In this case, transistor 12 is in the linear region until the pad terminal voltage (or output voltage V_o) 16 is lower than its PMOS threshold voltage V_t.

However, the use of digital impedance control include the disadvantages of step-like impedance adjustments (normally 5~10%), switching noise generation from turning on/off the different legs of the ODT resistor, interference with data transmission, and the need for a state machine in order to update resistor value.

In analog impedance control, the compensation is accomplished by changing the gate bias. However, the linearity of transistor 12 of Fig. 1 deteriorates when V_{GG} reaches approximately $V_{cc}/2$ at fast process corner and lower temperature. This is because transistor 12 enters the saturation region when the pad voltage is lower than $V_{cc}/2 + V_t$.

Based on the foregoing, there is a need for an improved ODT resistor suitable for analog impedance control, and an analog feedback loop that provides a suitable gate bias for the ODT resistor.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram of an active ODT resistor disclosed in prior art.

Fig. 2 is a circuit diagram of an ODT resistor in accordance with one embodiment of the present invention.

Fig. 3 is a graph illustrating the current as a function of voltage for an ODT resistor in accordance with one embodiment of the present invention in comparison with

a standard PMOS transistor.

Fig. 4 is a graph illustrating large signal resistance as a function of voltage for an ODT resistor in accordance with one embodiment of the present invention in comparison with a standard PMOS transistor and a prior art ODT resistor.

Fig. 5 is a graph illustrating the R-V characteristics for an ODT resistor at different process corners and temperature, with V_{cc}=1.2V.

Fig. 6 is a circuit diagram of an ODT resistor circuit that includes an ODT resistor and circuitry to control its gate bias based on process and temperature conditions in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

One embodiment of the present invention is an ODT resistor that has a poly resistor and three PMOS transistors. The ODT resistor is suitable for analog impedance control because it has improved linearity over all possible gate bias over all process corners and temperatures.

Fig. 2 is a circuit diagram of an ODT resistor 20 in accordance with one embodiment of the present invention. ODT resistor 20 is formed on a die of a semiconductor device that is placed on a PCB.

ODT resistor 20 includes three transistors 21-23 and a resistor 25. Resistor 25 is coupled to the source of transistor 21. Transistors 21-23 are PMOS transistors, with transistor 23 connected like a diode (i.e., the gate and source are coupled together). The gates of transistors 21 and 22 are coupled to a bias terminal 27. In another

embodiment, negative-channel metal-oxide semiconductor ("NMOS") transistors can be used in place of PMOS transistors 21-23.

Resistor 25 is a poly resistor that keeps transistor 21 from entering into the saturation region and therefore helps to make the I-V characteristics of ODT resistor 20 more linear. In another embodiment, if the requirement for linearity is not strict, resistor 25 can be a PMOS transistor with its gate connected to ground. In other embodiments, resistor 25 may be another type of resistor such as an Nwell, P diffusion or N diffusion resistor. The linearity of ODT resistor 20 is further improved by the current path formed by transistors 22 and 23. ODT resistor 20 can be turned off by applying V_{cc} (a power terminal of the silicon dye) to bias terminal 27. In one embodiment, bias terminal is coupled to the power supply (or ground if NMOS transistors are used) to provide stabilization.

Different resistance values can be obtained by changing the sizes of transistors 21-23 and resistor 25. In one embodiment, resistor 25 is chosen to be about 50% of the total resistance of ODT resistor 20.

In one embodiment, ODT resistor 20 provides 45 ohms of on-die termination in a 0.18um CMOS technology. In this embodiment, resistor 25 is 23 ohms, the channel width/channel length ratio ("W/L") for transistors 21, 22 and 23 are 210/0.28, 282/0.28 and 74/0.28 respectively.

In general, for a fixed ODT resistance, a bigger resistor 25 results in a better linearity of current-voltage characteristics. However, if resistor 25 is too big (e.g., 70% of the resistance of ODT resistor 20), the size of transistor 21 will be very big, and it is

hard to compensate the resistor 25 changes (caused by process/temperature variations) by adjusting gate bias 27

After the size of resistor 25 and transistor 21 are fixed, the size of transistors 22 and 23 may be adjusted to get the best R-V characteristics. To reduce the parasitic effect, transistor 23 should be kept as small as possible while transistor 22 can be very large.

Fig. 3 is a graph illustrating the current as a function of voltage (i.e., the I-V characteristics) for ODT resistor 20 (line 30) in accordance with one embodiment of the present invention in comparison with a standard PMOS transistor (line 32). The ODT resistor of line 30 is designed to provide a resistance of 45 ohms, has a Vcc=1.2V and T=85C for a typical process corner, and has a gate bias of 0.31V. As shown in Fig. 3, ODT resistor 20 as reflected in line 30 has a near perfect current-voltage characteristic like that of an ideal resistor, while the PMOS transistor, as reflected in line 32, has entered into deep saturation.

Fig. 4 is a graph illustrating large signal resistance as a function of voltage (i.e., the R-V characteristics) for ODT resistor 20 (line 33) in accordance with one embodiment of the present invention in comparison with a standard PMOS transistor (line 34) and the ODT resistor disclosed in Griffin (line 35). Within the Gunning Transistor Logic ("GTL") signal swing of 1.0V, the resistance from ODT resistor 20 is from 44 to 46 ohms, while for the ODT resistor disclosed in Griffin and the standard PMOS transistor, the large signal resistance is from 30.5 to 45.5 ohms, and from 23 to 68 ohms, respectively.

Fig. 5 is a graph illustrating the R-V characteristics for ODT resistor 20 at different process corners and temperature, with V_{cc}=1.2V. Line 40 is a fast process corner at 0C, line 41 a fast corner at 85C, line 42 a typical corner at 85C, and line 43 a slow corner at 110C. It can be seen that, except for a fast corner and 0C (line 40), the ODT resistance is within 45 ohms +/- 2ohms. The gate bias range is from 0.18V at a fast corner and 110C (line 43) to 0.47V at a fast corner and 0C (line 41).

Fig. 6 is a circuit diagram of an ODT resistor circuit 60 that includes an ODT resistor and circuitry to control its gate bias based on process and temperature conditions in accordance with one embodiment of the present invention. Resistor circuit 60 includes an ODT resistor that includes transistors 21-23 and resistor 25. Resistor circuit 60 further includes a high gain differential amplifier 50 and a high precision reference resistor 52 placed on the PCB board forming a feedback loop. The feedback loop constantly adjusts the bias voltage so that the ODT resistance is the same as the reference resistance. The accuracy of ODT resistance at half V_{cc} (across the ODT resistor) can be expressed as a function of differential amplifier 50 gain "A" and output voltage V_{out}:

$$R_{ODT}/R_{ref} = [1-2(V_{out}-V_{com})/V_{cc}]/[1+2(V_{out}-V_{com})/V_{cc}] \qquad (1)$$

Where V_{com} is the common mode output voltage of differential amplifier 50. Since the maximum V_{out} swing could be from V_{com} to 0V, or from V_{com} to V_{cc}-V_t, then for V_{com} =V_{cc}/2 and V_t<<V_{cc}, the upper and lower limits of the ODT resistance are determined by:

$$(1-1/A)/(1+1/A) < R_{ODT}/R_{ref} < (1+1/A)/(1-1/A) \qquad (2)$$

Where R_{ref} is the reference resistance on the PCB board. For A=500, equation (2) results in an ODT resistance that is within 0.4% of reference resistance.

The stability of the feedback loop is an issue in the design of the ODT resistor with analog impedance control. Various frequency compensation techniques can be used to avoid the loop oscillation. In one embodiment, a minimum phase margin of 45 degrees is used for stable operations. In this embodiment, an Nwell resistor (or MOS transistor) and a Miller capacitor are used for frequency compensation. A phase margin of 60 degrees is obtained.

As disclosed, an ODT resistor with analog impedance control in accordance with one embodiment of the present invention has a resistance value that is within +/- 5% across voltage swing range and process corners at operating temperature from 50C to 110C. This provides several advantages over digital impedance control. First, unlike the step-like impedance adjustments in digital control, the ODT resistor value in analog control can be continuously adjusted according to process and temperature conditions by changing the gate bias of the PMOS transistors. Second, analog impedance control does not generate noise. In contrast, with digital impedance control, the ODT resistance is adjusted by turning on and off different legs, and therefore generates spike-like noises on a power supply. Third, analog impedance control design does not interfere with data transmission and receiving. Finally, unlike with digital impedance control, a state machine is not required.

Several embodiments of the present invention are specifically illustrated and/or described herein. However, it will be appreciated that modifications and variations of

the present invention are covered by the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.